The Matrix Amplifier: A High-Gain Module for Multioctave Frequency Bands

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Abstract—**The characteristics of a new type of amplifier that makes simultaneous use of the additive and the multiplicative amplification process in one and the same module is discussed. The device, which achieves high-gain performance over multioctave bands, is a relative of the distributed amplifier. Initial experimental results demonstrated a small-signal gain of $G = 13.8 \pm 0.8$ dB with -11.4 dB of maximum return loss between 2.0 and 21.5 GHz when using MESFET's manufactured on ion-implanted substrate material and $G = 16.8 \pm 0.9$ dB gain over the 2.3–20.3-GHz frequency band in the case of vapor-phase-epitaxial material. The principle, the theory, and the experimental results are discussed in detail.**

I. Introduction

AMPLIFICATION from two or more active devices may be classified as multiplicative or additive. In the case of the former, the overall gain is proportional to the product of the gains supplied by the individual modules, while in the case of the latter it is proportional to the sum of the powers contributed by the individual active devices. The vast majority of amplifiers make use of the multiplicative process through cascading. The most prominent exception is the distributed or traveling-wave amplifier whose amplifying mechanism is based on the additive principle [1], [2]. While in most practical applications the latter produces less gain per device than the multiplicative amplifier types, it yields significantly larger bandwidths through the ingenious use of the active devices' parasitics. Since 1937, when the invention of the distributed amplifier was patented [1], very few modifications of the original concept have surfaced. However, two variations have recently emerged that are of practical importance. In the first, the common source MESFET is replaced by a cascaded two-port that consists of a common-source first stage followed by a common-gate second stage separated by a two-port that serves as an interstage transformer [3]. This type of amplifier produces moderately higher gains and significantly higher reverse isolations. In the second modification, two distributed-amplifier circuits are paralleled by establishing a common drain line. The input signal is divided and applied to the two input terminals of the ensuing network while the output signal is extracted at the common drain terminal [4]. In this case, the output power is doubled with no change in gain.

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In this paper, a circuit is described that adds a new dimension to the distributed amplifier in the form of one or more rows of transistors, i.e., active tiers. In its most general form, the new amplifier consists of an array of m rows and n columns of active devices. Each column is linked to the next by inductors or transmission-line elements connected at the input and output terminals of each transistor, composing a lattice of circuit elements. For m active tiers, there are $2m$ idle ports that are terminated into power-dissipating loads. The purpose of adding the vertical dimension to the horizontal dimension of the distributed amplifier in the form of the $m \times n$ rectangular array is to combine the multiplicative and additive amplification process in one and the same module. The advantages of the new device include significantly higher gain and reverse isolation over wide bandwidths at considerably reduced size. Due to its regular geometrical arrangement of circuit elements, very much similar to the rectangular array of mathematical elements in a matrix, we propose to designate the new device the matrix amplifier.

II. The Principle

The concept of the matrix amplifier combines the processes of additive and multiplicative amplification in one and the same module. Its purpose, therefore, is to combine the characteristic features of both principles, namely, to increase the gain of the additive amplifier concept and the bandwidth of the multiplicative amplifier concept. This can be accomplished in a module whose size is significantly reduced when compared with the traditional amplifier types of similar gain and bandwidth performance.

The principle of the matrix amplifier is most easily explained by means of a simplified schematic making use of an idealized transistor model. The latter consists of an input (C_{gs}), an output shunt capacitance (C_{ds}), and a current generator that is controlled by the input voltage. Its equivalent circuit is shown in Fig. 1 along with a schematic of this stripped-down version of the matrix amplifier in the form of a 2×4 array.

Each link of the input and output artificial transmission line consists of the input and the output shunt capacitances $C = C_{gs} + C_{ds}$ and the inductance $1/2\ L$. Choosing $C = C_{gs} + C_{ds}$ makes all three artificial transmission lines

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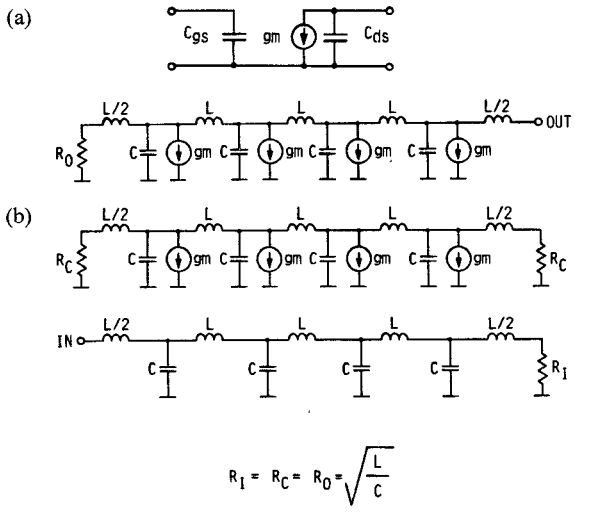


Fig. 1. (a) The idealized transistor model and (b) the schematic of an elementary version of the matrix amplifier in form of a 2×4 array.

of the amplifier in Fig. 1 identical and requires adding shunt capacitance other than that inherent in the devices to the gate line and the drain line, but none to the center line. The idle gate and drain ports are terminated with a resistor that equals the characteristic impedances of their respective artificial transmission lines. In contrast, both idle ports of the center line are terminated into the arbitrary resistor R_c. Since the idealized circuit in Fig. 1(b) has no feedback path between the transmission lines and, in addition, employs identical artificial transmission lines on both sides of the center line, the input and output reflection coefficients are identical and independent of the characteristics of the center transmission line and its terminations. It should be pointed out, however, that this condition no longer exists as soon as the idealized transistors are replaced by real devices which have parallel and series feedback, as well as input and output admittances that cannot be made identical by attaching additional circuit elements.

The relationship between the input and output voltages and currents of an elementary module as displayed in Fig. 1(b) and consisting of n links may be expressed by the quadratic matrix

where

$$\Omega = \omega\sqrt{LC} \tag{1a}$$

and

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1b}$$

are the normalized frequency and the characteristic impedance of the artificial input and output transmission lines, respectively. The voltages and currents are measured at the input of the drain line (V_{D0}, I_{D0}), the center line (V_{C0}, I_{C0}), and the gate line (V_{G0}, I_{G0}) and at the ports of the respective output lines ($V_{Dn}, I_{Dn}, V_{Cn}, I_{Cn}, V_{Gn}, I_{Gn}$). If we now terminate the idle ports in accordance with the schematic of Fig. 1(b), i.e.,

$$V_{Gn} = -Z_0 I_{Gn} \tag{1c}$$

$$V_{D0} = -Z_0 I_{D0} \tag{1d}$$

$$V_{C0} = -R_C I_{C0} \tag{1e}$$

$$V_{Cn} = -R_C I_{Cn} \tag{1f}$$

and further assume that our matrix amplifier has $n = 4$ links, we find four frequencies for which the input and output reflection coefficients are zero, namely $\Omega = 0$, $\Omega = \sqrt{2-\sqrt{2}}$, $\Omega = \sqrt{2}$, and $\Omega = \sqrt{2+\sqrt{2}}$. The S-parameters for the first and the third normalized frequency can be easily determined with (1). They are, for $\Omega = 0$,

$$S_{11} = S_{22} = 0 \tag{2a}$$

$$S_{12} = 0 \tag{2b}$$

$$S_{21} = \left(\frac{n}{2}\right)^2 R_C/Z_0(g_m Z_0)^2 \tag{2c}$$

and for $\Omega = \sqrt{2}$ and $n = 4$,

$$S_{11} = S_{22} = 0 \tag{2d}$$

$$S_{12} = 0 \tag{2e}$$

$$S_{21} = \left[4\frac{R_C}{Z_0} + \frac{Z_0}{R_C} + j\frac{1}{2}\sqrt{2}\right](g_m Z_0)^2. \tag{2f}$$

At $\Omega = 0$, we have the case of n devices in parallel, resulting in a simple expression for the S_{21}-parameter. For $\Omega = \sqrt{2}$, the S_{21}-parameter for $n = 4$ (2f) is very much dependent on R_C/Z_0 and approaches infinity for R_C/Z_0

$$\begin{bmatrix} V_{D0} \\ I_{D0} \\ V_{C0} \\ I_{C0} \\ V_{G0} \\ I_{G0} \end{bmatrix} = \left[\begin{array}{cc|cc|cc} \left(1-\frac{1}{2}\Omega^2\right) & j\Omega Z_0\left(1-\frac{1}{4}\Omega^2\right) & j\frac{1}{2}\Omega Z_0 g_m & -\frac{1}{4}\Omega^2 Z_0^2 g_m & 0 & 0 \\ j\frac{\Omega}{Z_0} & \left(1-\frac{1}{2}\Omega^2\right) & g_m & j\frac{1}{2}\Omega Z_0 g_m & 0 & 0 \\ \hline 0 & 0 & \left(1-\frac{1}{2}\Omega^2\right) & j\Omega Z_0\left(1-\frac{1}{4}\Omega^2\right) & j\frac{1}{2}\Omega Z_0 g_m & -\frac{1}{4}\Omega^2 Z_0^2 g_m \\ 0 & 0 & j\frac{\Omega}{Z_0} & \left(1-\frac{1}{2}\Omega^2\right) & g_m & j\frac{1}{2}\Omega Z_0 g_m \\ \hline 0 & 0 & 0 & 0 & \left(1-\frac{1}{2}\Omega^2\right) & j\Omega Z_0\left(1-\frac{1}{4}\Omega^2\right) \\ 0 & 0 & 0 & 0 & j\frac{\Omega}{Z_0} & \left(1-\frac{1}{2}\Omega^2\right) \end{array}\right]^n \begin{bmatrix} V_{Dn} \\ -I_{Dn} \\ V_{Cn} \\ -I_{Cn} \\ V_{Gn} \\ -I_{Gn} \end{bmatrix} \tag{1}$$

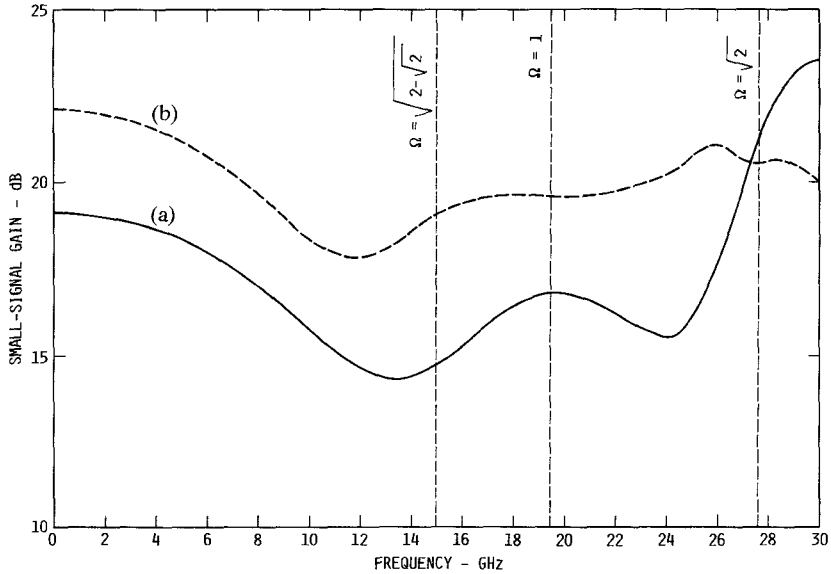


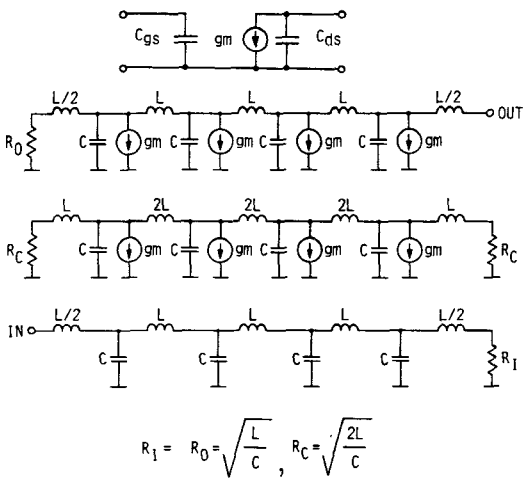
Fig. 2. Small-signal gain of (a) the 2×4 array of Fig. 1 for $g_m = 30$ mS, $C = 0.163$ pF, $L = 0.4075$ nH, and $R_C = Z_0 = 50\ \Omega$ and of (b) the 2×4 array in Fig. 3 for $g_m = 30$ mS, $C = 0.163$ pF, $L_G = L_D = 0.4075$, $L_C = 0.815$ nH, and $R_C = \sqrt{2}\,Z_0 = 70.7\ \Omega$.

$= 0$ and $R_C/Z_0 = \infty$. Minimum gain $|S_{21}|^2$ occurs at $R_C/Z_0 = 1/2$, while minimum gain variation across the frequency band is found at $R_C/Z_0 = 1$. Curve (a) of Fig. 2 displays the frequency response of the amplifier's gain for $n = 4$, $g_m = 30$ mS, $C = 0.163$ pF, $L = 0.4075$ nH, and $R_C = Z_0 = 50\ \Omega$. The capacitance $C = C_{gs} + C_{ds}$ and the transconductance g_m are taken from S-parameter measurements of the device that will be later used in our experiments and whose equivalent circuit is shown in Fig. 9. Since, except for C_{gs} and C_{ds}, all other parasitics that characterize our active device have been removed, the gain response of our idealized amplifier (Fig. 1), of course, extends far beyond the frequencies that the actual GaAs MESFET is able to cover. We will see in the next section that the upper limit of the frequency band when using practical devices is located somewhere between $\Omega = 1$ and $\Omega = \sqrt{2}$. For this reason, we have determined the S-parameters of the 2×4 array of Fig. 1 at $\Omega = 1$. They are, for $\Omega = 1$ and $n = 4$,

$$S_{11} = S_{22} = \frac{-j}{4 + j7} \tag{2g}$$

$$S_{12} = 0 \tag{2h}$$

$$S_{21} = -\frac{4}{(1 + j7/4)^2} \cdot \left[2\frac{[(R_C/Z_0 + 1/4) + j(R_C/Z_0 + 1)]^2}{R_C/Z_0 + j\left(\left(\frac{R_C}{Z_0}\right)^2 + 3/4\right)} - (1 + j9/4) \right] (g_m Z_0)^2. \tag{2i}$$



$$R_1 = R_0 = \sqrt{\frac{L}{C}}, \quad R_C = \sqrt{\frac{2L}{C}}$$

Fig. 3. Schematic of an elementary version of the matrix amplifier with double inductance ($2L$) in the center line.

The gain and the gain flatness of our idealized amplifier (Fig. 1) can be improved by doubling the inductance of the links in the center line in accordance with the circuit of Fig. 3. Since no changes were made in either the gate or the drain transmission line, the input and output reflection coefficients are again zero at $\Omega = 0$, $\Omega = \sqrt{2 - \sqrt{2}}$, $\Omega = \sqrt{2}$, and $\Omega = \sqrt{2 + \sqrt{2}}$.

In the case of $\Omega = 0$, the S-parameters are identical to those of (2a)–(2c), while for $\Omega = \sqrt{2}$ (and $n = 4$) they are expressed by

$$S_{11} = S_{22} = 0 \tag{3a}$$

$$S_{12} = 0 \tag{3b}$$

$$S_{21} = -\frac{12R_C/Z_0 + j7\sqrt{2}}{1 - j2\sqrt{2}\,R_C/Z_0}(g_m Z_0)^2. \tag{3c}$$

From (3), it becomes immediately apparent that in contrast to the circuit of Fig. 1 the gain of the circuit in Fig. 3 is finite for $R_C/Z_0 = 0$ and $R_C/Z_0 = \infty$. As can be seen

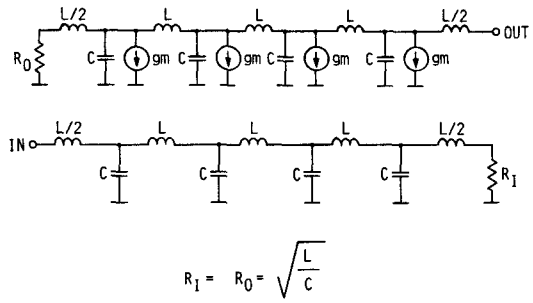


Fig. 4. Schematic of a simplified distributed amplifier.

from curve (b) in Fig. 2 for $n = 4$, $g_m = 30$ mS, $C = 0.163$ pF, $L = 0.4075$ nH, and $R_C/Z_0 = \sqrt{2}$, both the average gain and the total gain variation between $\Omega = 0$ and $\Omega = \sqrt{2}$, even though not ideal, have significantly improved over those of the circuit in Fig. 1.

In order to dramatize the dual nature, i.e., multiplicative and additive amplification characteristics, of the matrix amplifier, a comparison of its S-parameters at certain frequencies with those of an equivalent distributed amplifier follows. The schematic of the latter is shown in Fig. 4. Again, for $\Omega = 0$ and $\Omega = \sqrt{2}$, the input and output reflection coefficients are zero. However, the input and output shunt capacitances are now $C = C_{gs}$ (if $C_{gs} > C_{ds}$) or $C = C_{ds}$ (if $C_{ds} > C_{gs}$), which, in accordance with (1b), results in a lower inductivity L ($Z_0 = 50$ Ω) and, therefore, in a slightly higher bandwidth. The S-parameters of the idealized distributed amplifier in Fig. 4 at the normalized frequencies $\Omega = 0$ and $\Omega = \sqrt{2}$ are, for $\Omega = 0$,

$$S_{11} = S_{22} = 0 \tag{4a}$$

$$S_{12} = 0 \tag{4b}$$

$$S_{21} = -1/2ng_mZ_0 \tag{4c}$$

and for $\Omega = \sqrt{2}$ and $n = 4$

$$S_{11} = S_{22} = 0 \tag{4d}$$

$$S_{12} = 0 \tag{4e}$$

$$S_{21} = -3g_mZ_0. \tag{4f}$$

A comparison of (2c) with (4c) and of (2f) with (4f) clearly shows the multiplicative property of the matrix amplifier, which is reflected in the term $(g_mZ_0)^2$.

In order to compare the performance of a matrix amplifier of n links and m multiplicative tiers ($n = 4$ and $m = 2$ in Figs. 1 and 3) with an equivalent distributed amplifier, the latter has to consist of n links and m cascaded stages. Such a comparison, however, is not very meaningful when performed for the idealized cases we have treated so far. It will be performed later when we describe the matrix amplifier's performance based on actually measured devices. The purpose, then, of what has been discussed until now is merely to demonstrate the dual nature of the matrix amplifier's functions, i.e., additive and multiplicative amplification in one and the same module.

III. Design Considerations

A. Analytical Tools

In the preceding, we explained the principle of the matrix amplifier by means of a highly simplified model of

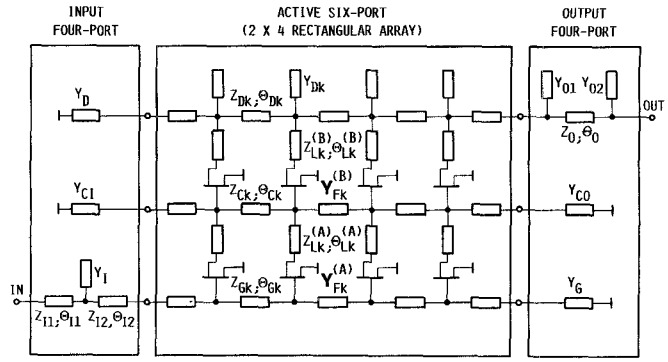


Fig. 5. Major circuit blocks of the matrix amplifier (2×4 array) in its unabridged form.

a 2×4 array, i.e., a four-link device with two multiplicative gain tiers. While the principle generally allows use of any number of links and multiplicative gain tiers, we will proceed with the example of the 2×4 array. The schematic of the matrix amplifier incorporating the actual circuit elements is shown in Fig. 5. It consists of three major blocks, i.e., the active six-port flanked by the input and the output four-port.

The active six-port incorporates the transistors characterized by their sets of Y-parameters, the network of inductances (not shown in Fig. 5) or transmission-line elements represented by their respective characteristic impedances and line lengths, and the open-circuit shunt stubs capacitively loading the drain line. In contrast, the input and output four-ports contain only passive circuit elements, i.e., the terminations of the amplifier's idle ports and a simple input and output matching network. In what follows, we will attempt to formulate a number of matrix equations that are useful to compute the characteristics of the amplifier. As mentioned earlier, the analysis will be performed by means of the 2×4 array shown in Fig. 5, but may be expanded to m multiplicative tiers, resulting in square matrices composed of $(2m+2)^2$ elements. In the case of the 2×4 array analyzed here, we have $m = 2$ tiers, leading to a set of 6×6 matrices which when multiplied make it possible to compute the input and output voltages and currents of our device. The equation describing the voltages and currents of a matrix amplifier consisting of p elementary six-ports is of the form

$$\begin{bmatrix} V_{D0} \\ I_{D0} \\ V_{C0} \\ I_{C0} \\ V_{G0} \\ I_{G0} \end{bmatrix} = \prod_{k=0}^{k=p} A_k \begin{bmatrix} V_{Dn} \\ -I_{Dn} \\ V_{Cn} \\ -I_{Cn} \\ V_{Gn} \\ -I_{Gn} \end{bmatrix}. \tag{5}$$

Here, as in (1), subscripts $(\ )_0$ and $(\ )_n$ indicate the input and output quantities, respectively. The matrix (5) results from the multiplication of all matrices $[A_k]$ that characterize the elementary six-ports which have been cascaded between the terminals of the amplifier. For example, the characteristics of the two-tier active six-port of Fig. 6 are represented in the matrix (A1) of the Appendix. Similarly, those of the transmission-line elements in Fig. 7(a) are

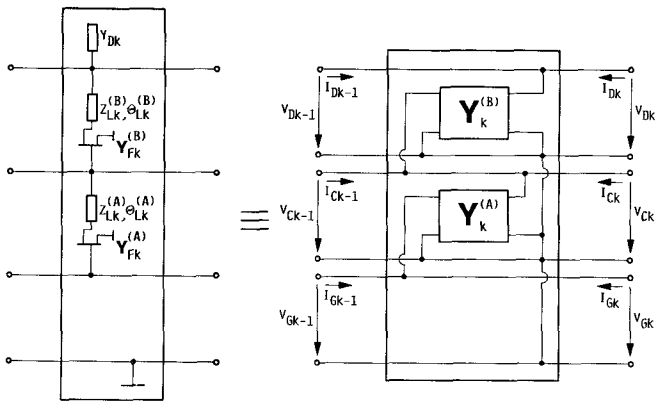


Fig. 6. The two-tier active six-port.

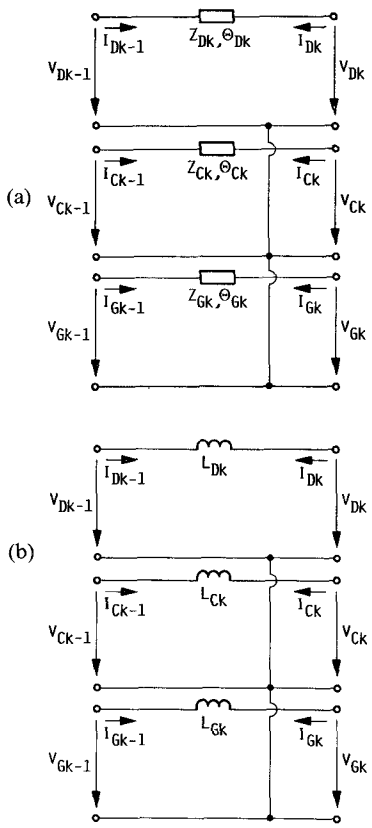


Fig. 7. The six-port links using (a) transmission-line elements or (b) inductors.

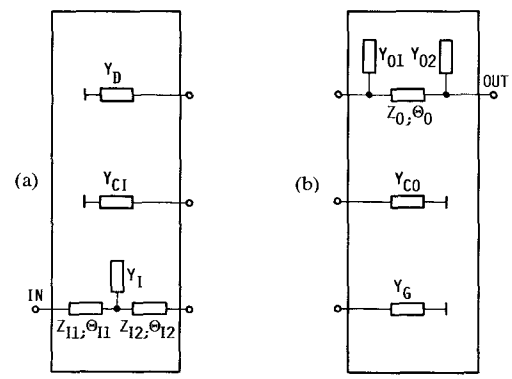


Fig. 8. The (a) input and (b) output four-ports.

reflected in the matrix (A2), while those of the inductive links in Fig. 7(b) may be determined with (A3). Finally, the characteristics of the input and output four-ports in Fig. 8(a) and (b) are expressed by the matrices (A4) and (A5), respectively.

Once the idle ports of the amplifier are terminated in accordance with Fig. 5 and the matrices of all elementary six-ports have been multiplied in the sequence they are cascaded, the resulting matrix equation may be reduced to that of a two-port:

$$\begin{bmatrix} I_{G0} \\ I_{Dn} \end{bmatrix} = \begin{bmatrix} Y_{11}^{(MA)} & Y_{12}^{(MA)} \\ Y_{21}^{(MA)} & Y_{22}^{(MA)} \end{bmatrix} \begin{bmatrix} V_{G0} \\ V_{Dn} \end{bmatrix}. \tag{6}$$

The admittance parameters $Y_{ij}^{(MA)}$ of this two-port (A7) are presented in the Appendix. They can be used to formulate the gain, the reflection coefficients, and the reverse isolation of the amplifier. As to the involvement of multiplying a great number of matrices of the complexity represented by (A1)–(A5), when actual MESFET's are employed, the computer greatly simplifies this task. The computations, of course, can be executed with the commercially available computer programs that are based on nodal analysis.

The use of equations (A1)–(A7) leads us to the exact solution of the admittance parameters; however, their complexity gives us no immediate clue to the amplification principle of the device. To obtain a descriptive set of Y-parameters, we take a very brief look at the amplifier's low-frequency model. At low frequencies, where the internal feedback of the transistors and the influence of the linking elements may be neglected (in our case, $f \leqslant 2$ GHz), the expressions of the admittance parameters (A7) take the simple and interpretive form

$$Y_{11}^{(MA)} \approx Y_G + nY_{11}^{(A)} \tag{7a}$$

$$Y_{12}^{(MA)} \approx 0 \tag{7b}$$

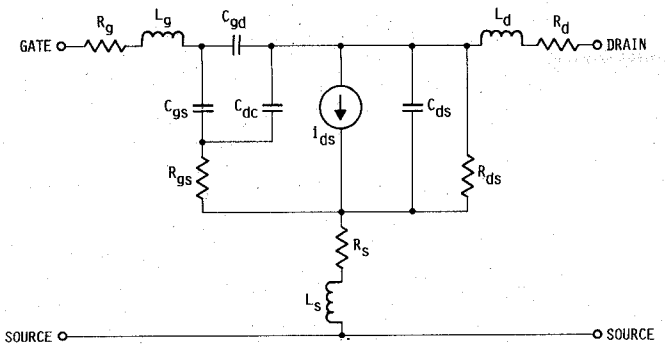
$$Y_{21}^{(MA)} \approx -\frac{n^2 Y_{21}^{(A)} Y_{21}^{(B)}}{Y_{CI} + Y_{C0} + n\left(Y_{11}^{(B)} + Y_{22}^{(A)}\right)} \tag{7c}$$

$$Y_{22}^{(MA)} \approx Y_D + nY_{22}^{(B)}. \tag{7d}$$

B. Effects of the Device Parasitics

Let us now take a closer look at a simple 2×4 array identical to that shown in Fig. 1(b) in which the idealized active device is replaced by a GaAs MESFET characterized by the equivalent-circuit elements shown in Fig. 9. They are based on S-parameter measurements performed on a transistor incorporating a 0.25×200-μm gate having a peak doping of 5.7×10^{17} cm^{-3}. The data are representative of the devices that were used in our experimental amplifiers.

The computed gains are plotted in curve (a) of Fig. 10 for the case where all inductive links are identical, as in the circuit of Fig. 1(b). Comparing the curves (a) in Fig. 2 and Fig. 10 reveals the immense influence that the parasitics of the GaAs MESFET's exert on the module's gain performance. Not only has the circuit's small-signal gain been significantly affected; in addition, its bandwidth has suffered severely. Obviously, this comparison renders our



INTRINSIC ELEMENTS			EXTRINSIC ELEMENTS		
gm	=	29.7 mS	R_g	=	5.1 ohm
τ_0	=	1.2 psec	L_g	=	.152 nH
C_{gs}	=	.1385 pF	R_s	=	.5 ohm
C_{gd}	=	.015 pF	L_s	=	.034 nH
C_{dc}	=	.033 pF	C_{ds}	=	.023 pF
R_{gs}	=	4.0 ohm	R_d	=	1 ohm
R_{ds}	=	213 ohm	L_d	=	.434 nH

Fig. 9. Equivalent circuit and circuit elements of the GaAs MESFET.

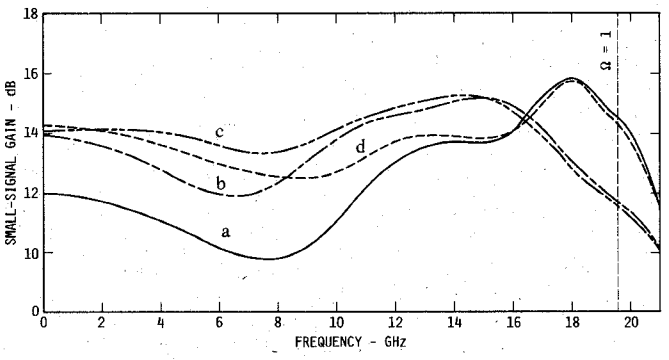


Fig. 10. Small signal gain of the 2×4 array when employing the device of Fig. 9 and the four following sets of values for the circuit components: (a) $L_G = L_C = L_D = 0.4075$ nH, $C_G = C_C = 0$, $C_D = 0.1385$ pF ($C = 0.163$ pF), $R_G = R_{C1} = R_{C2} = R_D = 50$ Ω; (b) $L_G = 1/2\ L_C = L_D = 0.4075$ nH, $C_G = C_C = 0$, $C_D = 0.1385$ pF ($C = 0.163$ pF), $R_G = R_D = 50$ Ω, $R_{C1} = R_{C2} = 70.7$ Ω; (c) $L_G = 1/2\ L_C = L_D = 0.4325$ nH, $C_G = C_C = 0$, $C_D = 0.105$ pF, $R_G = 37$ Ω, $R_D = 90$ Ω, $R_{C1} = 135$ $R_{C2} = 50$ Ω; (d) $L_G = L_C = L_D = 0.385$ nH, $C_G = C_C = 0$, $C_D = 0.081$ pF, $R_G = 30$ Ω, $R_D = 110$ Ω, $R_{C1} = 325$ Ω, $R_{C2} = 50$ Ω.

study of the simplified circuit in the previous section a qualitative analysis at best. However, as stated previously, the intent was to demonstrate in descriptive terms the matrix amplifier's dual nature. A similar discrepancy becomes apparent when we compare the circuits that use twice the inductance in the center line in accordance with Fig. 3. Again, the small-signal gain and the bandwidth experience a significant decline due to the transistors' parasitic elements, as demonstrated by curves (b) in Figs. 2 and 10. The gain variation of the simple circuits represented by the schematics in Figs. 1 and 3, however, may be improved by altering the inductors linking the active devices.

C. Performance Improvements

The gain variations produced by the simple circuits represented by the schematics of Figs. 1 and 3 after the

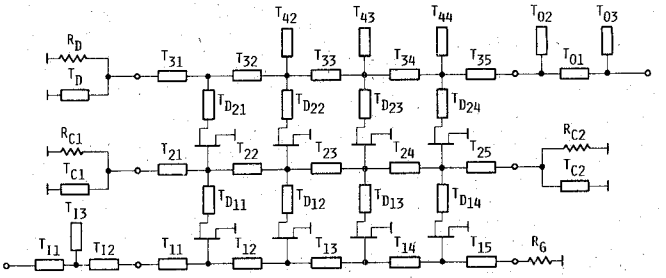


Fig. 11. Schematic of the experimental amplifier. T_{In} denotes input-matching transmission-line elements; T_{On} output-matching transmission-line elements; T_{1n} gate-line transmission-line elements; T_{2n} center-line transmission-line elements; T_{3n} drain-line transmission-line elements; T_{D1n} transforming transmission-line elements (1. tier); T_{D2n} transforming transmission-line elements (2. tier); T_{4n} drain-line open-circuit shunt stubs; R_G gate-line termination; R_{Cn} center-line terminations; R_D drain-line termination; T_{Cn} center-line short-circuit shunt stubs; T_D drain-line short-circuit shunt stub.

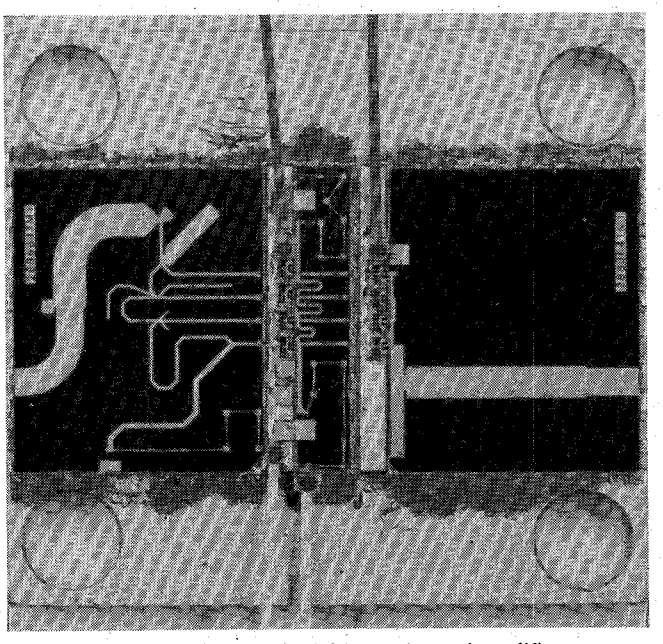


Fig. 12. Photograph of the experimental amplifier.

idealized devices (Fig. 1(a)) have been replaced by practical GaAs MESFET's (Fig. 9) are not acceptable and need improvement. Simple adjustments in the values of the idle ports' terminations, the linking inductors, and the loading capacitors produce the changes displayed by the gain patterns of curves (c) and (d) of Fig. 10.

If, however, a further enhancement of performance is desired, the principle of the identical six-port elements has to be abandoned, i.e., all linking elements as well as all capacitive loads need to be subjected to individual optimization. Furthermore, simple input and output matching networks must be added to improve the matrix amplifier's input and output matches. In addition, it becomes necessary to insert series inductive elements, i.e., inductors or high-impedance transmission-line elements between the drain terminals of the active devices and their respective linking elements.

Fig. 11 shows the schematic of the resulting 2×4 matrix amplifier whose practical realization is reflected in the photograph of Fig. 12. The amplifier employes the device characterized by the equivalent circuit and its elements of

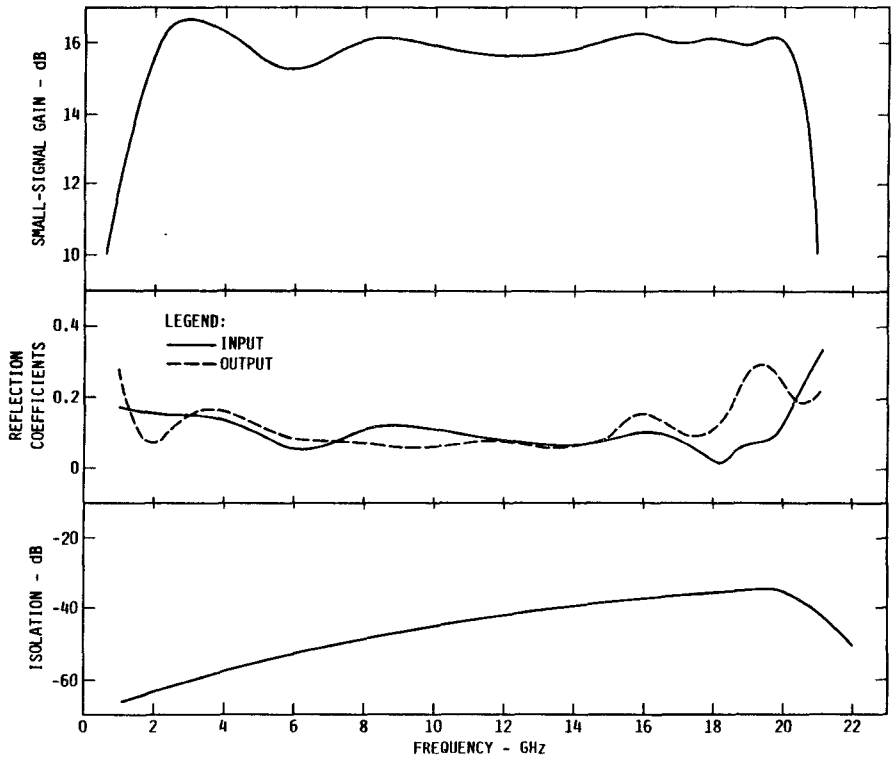


Fig. 13. Computed performance characteristics of the experimental amplifier (Fig. 11).

Fig. 9. It can be seen from the photograph that, due to the optimization applied to all circuit elements, hardly any are identical in length when compared to their peers located in equivalent positions. The module's computed small-signal gain, reflection coefficients, and reverse isolation are shown in Fig. 13. A comparison with the gain curves (d) for identical links in Fig. 10 reveals significant improvements in both absolute gain and the amount of gain variation, justifying the effort of individual-circuit-element optimization [5].

Since cascading two distributed amplifiers also combines the gain of each module through multiplication, it is of considerable interest how the performance of our 2×4 matrix amplifier compares to a unit consisting of two cascaded distributed amplifier modules using the same number and type of transistors. In order to achieve a meaningful comparison, all circuit elements of each of the identical stages are individually optimized to produce the best two-stage amplifier performance. The results are plotted in Fig. 14. Comparing the data of Fig. 13 with those of Fig. 14 clearly shows that while both amplifiers have similar gain levels, the gain variation and the bandwidth of the two-stage amplifier, as expected, are superior. However, the input and output reflection coefficients of the matrix amplifier exhibit somewhat lower levels than those of the two-stage unit. In contrast to the moderate improvements of the reflection coefficients computed for the matrix amplifier over those of the two-stage distributed amplifier, measured data decisively demonstrate the better performance of the 2×4 array. On the basis of the above data comparison alone, it is hard to justify the existence of the matrix amplifier. However, when drawing a comparison between the sizes of the two units, the matrix amplifier has the clear edge. The overall circuit area is approximately 65 percent that of the two-stage amplifier. This is a significant advantage wherever size and, for monolithic devices, cost are of great importance. In addition, better noise figures may be expected by using the new principle. The theoretical proof will be presented in a forthcoming paper. The high concentration of active devices in the center section of the matrix amplifier, as shown in Fig. 12, makes this portion of the circuit especially suitable and, due to the fact that it occupies only a small fraction of the entire amplifier, very cost-effective for monolithic technology. The area-consuming drain-line circuitry may then be fabricated on substrate material other than GaAs, which retains the option of tuning for this sensitive part of the amplifier.

IV. Experimental Results

A photograph of the experimental matrix amplifier is shown in Fig. 12. The overall circuit size is 0.500×0.240 in, and 10-mil-thick quartz was used for substrate material. The unit is self-biased and only one dc voltage (12 V) was supplied to a simple voltage divider which, in our experimental unit, is located outside the amplifier housing. The sum of all drain currents totaled 304 mA. The amplifier's small-signal gain, return losses, and reverse isolation are plotted in Fig. 15. From 2.0 GHz to 21.5 GHz, the small-signal gain is $G=13.8\pm0.8$ dB, with a worst return loss of -11.7 dB for the input port and -11.4 dB for the output port. The reverse isolation ranges from a minimum of -33.2 dB to a maximum of -66 dB across the 19.5-GHz band. For comparison, the computed small-signal gain (Fig. 13) is $G=15.9\pm0.7$ dB over the slightly narrower 2–20.0-GHz frequency band. A maximum noise figure of

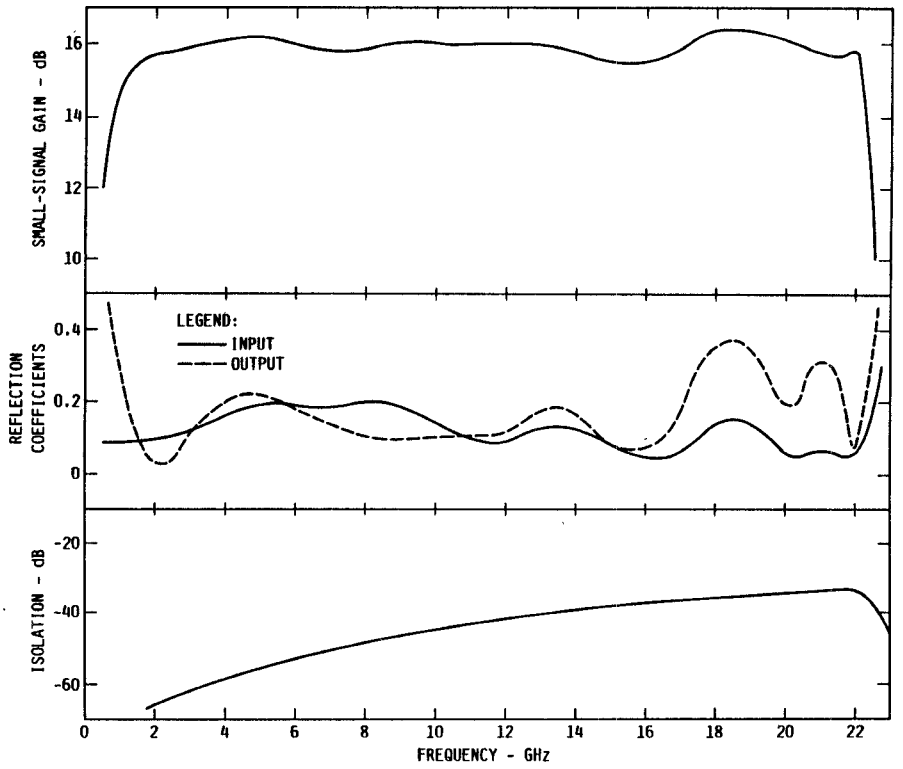


Fig. 14. Computed performance characteristics of an optimized two-stage distributed amplifier.

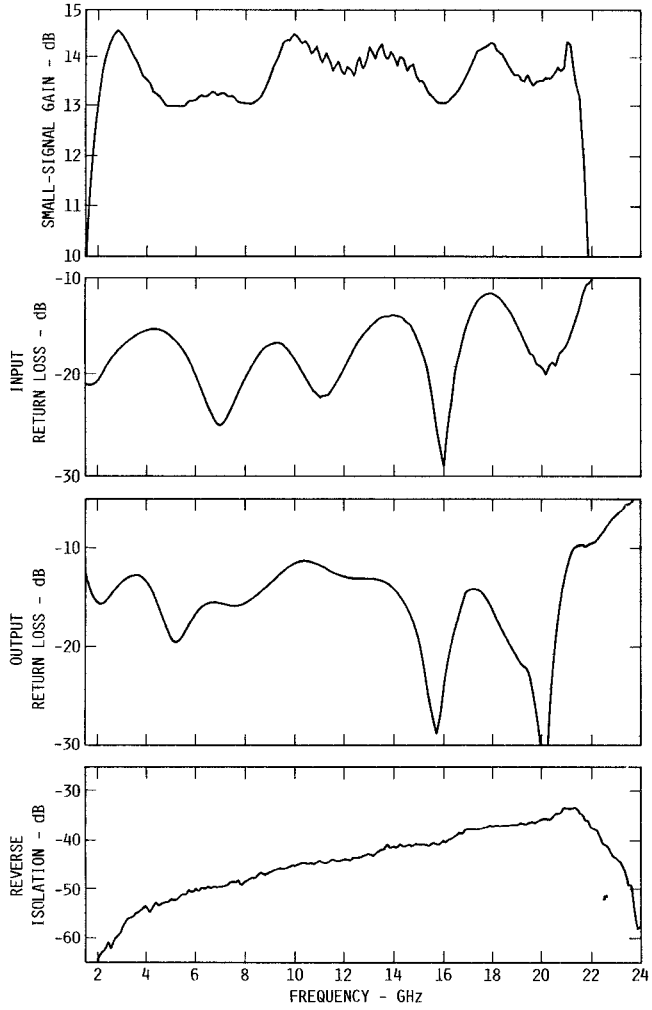


Fig. 15. Measured performance of the experimental amplifier employing MESFET's manufactured on ion-implanted material.

NF = 8.0 dB between 2.0 GHz and 20.0 GHz and a minimum output power of 17.0 dBm at the 1-dB compression points between 2.0 GHz and 21.0 GHz were measured. The amplifier's large-signal gain at 100 mW of output power is $G = 11.6 \pm 1.5$ dB from 2 GHz to 21 GHz. The maximum harmonic output power at the 1-dB compression points is generated by the first harmonic and is 21 dB below the fundamental output power at $f_0 = 2$ GHz. As shown in Fig. 16, subsequent amplifiers incorporating GaAs MESFET's fabricated with the same mask set but on vapor-phase-epitaxial rather than ion-implanted material yield $G = 16.3 \pm 0.9$ dB of small-signal gain over the slightly narrower 2.3–20.3-GHz frequency band using the same basic circuit of Fig. 12. A maximum noise figure of NF = 6.6 dB was measured between 2.5 GHz and 18 GHz and NF = 5.1 dB from 8 GHz to 18 GHz. In contrast to the ion-implanted substrate's peak doping of $N = 6 \times 10^{17}$ cm^{-3} at a depth of 0.1 μm, the vapor-phase-epitaxial substrate's doping is $N = 4 \times 10^{17}$ cm^{-3} with a 90-percent level at a depth of 0.2 μm. [6]

V. Conclusions

A new type of amplifier has been described which combines the process of additive with that of multiplicative amplification. The principle of operation has been explained by means of a simple circuit employing idealized transistors. Based on a rigorous solution for voltages and currents involving GaAs MESFET's with 0.5×200-μm gate dimensions, the characteristics of the amplifiers were examined employing a 2×4 array as a typical example. In pursuit of an acceptable performance, all circuit parameters were subjected to an optimization routine. Based on these computed results, a matrix amplifier consisting of the

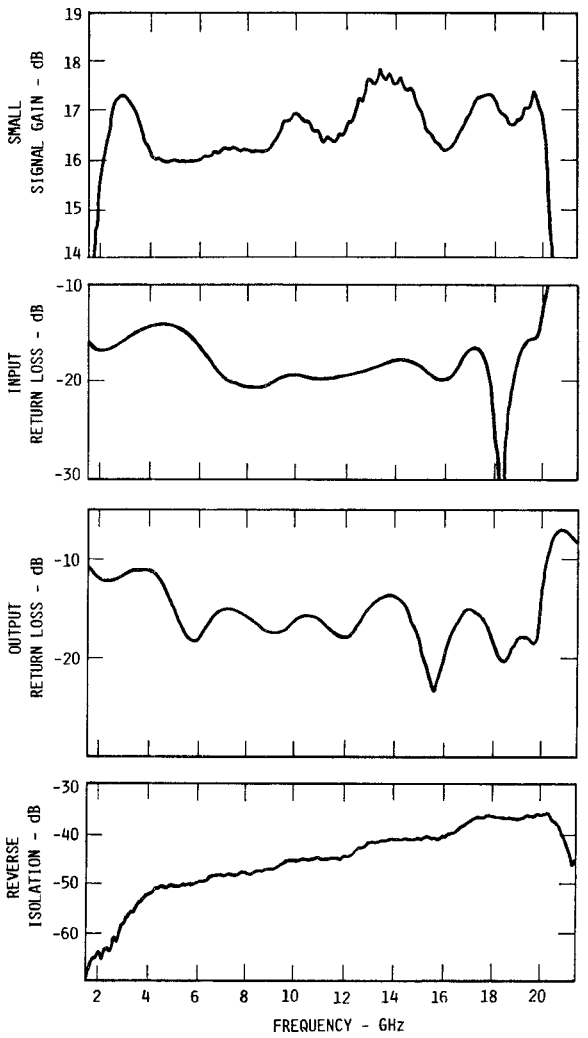


Fig. 16. Measured performance of the experimental amplifier using MESFET's manufactured on vapor-epitaxial material.

aforementioned 2×4 array was designed and fabricated. Subsequent measurements clearly demonstrated the feasibility of the new concept. Measured gain performance is approximately what one would expect from two cascaded distributed amplifiers whose performance is optimized as a single unit. The advantages of the matrix amplifier over the cascaded distributed amplifier are size and cost, especially when monolithic technology is used. In addition, better reflection coefficients and noise figures may be expected from the new device. Besides higher gain, the advantage of the matrix amplifier over the distributed amplifier employing the cascade-connected devices [3] is the ability to separately bias each row of devices by means of the linking elements. Due to the initial encouraging results and the vast number of options offered by the new concept, the 2×4 array described here may be only the first representative of an emerging class of amplifiers.

Appendix
Voltages, Currents, and Y-Parameters of the Two-Tiered Matrix Amplifier

The circuit shown in the schematic of Fig. 5 serves as a representative example of a matrix amplifier that contains $m = 2$ tiers of active devices. For ease of a rigorous analysis, it is expedient to divide this network into subcircuits that can be represented by relatively uncomplicated equations for the voltages and the currents at the terminals of the ensuing six-ports. For convenience, we have chosen five types of six-ports that satisfy the requirements imposed by the possible subcircuits of the matrix amplifier in Fig. 5. They are the two-tier active six-port of Fig. 6, the six-port links composed of transmission-line elements or inductors of Fig. 7(a) and (b), and, finally, the input and output four-ports of Fig. 8(a) and (b), respectively. Each of the described six-ports may be represented by a quadratic matrix. Following the above order, the matrix equation of the two-tiered active six-port is

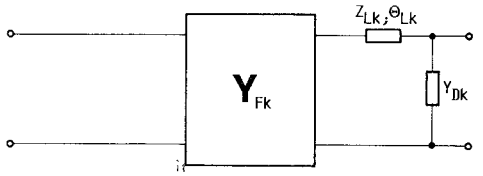


Fig. 17. Active device with output transformer and capacitive load.

$$\begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ \hline V_{Ck-1} \\ I_{Ck-1} \\ \hline V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = \left[\begin{array}{cc|cc|cc} 1 & 0 & 0 & 0 & 0 & 0 \\ Y_{22k}^{(B)} & 1 & Y_{21k}^{(B)} & 0 & 0 & 0 \\ \hline 0 & 0 & 1 & 0 & 0 & 0 \\ Y_{12k}^{(B)} & 0 & \left(Y_{11k}^{(B)} + Y_{22k}^{(A)}\right) & 1 & Y_{21k}^{(A)} & 0 \\ \hline 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & Y_{12k}^{(A)} & 0 & Y_{11k}^{(A)} & 1 \end{array}\right] \cdot \begin{bmatrix} V_{Dk} \\ -I_{Dk} \\ \hline V_{Ck} \\ -I_{Ck} \\ \hline V_{Gk} \\ -I_{Gk} \end{bmatrix}. \tag{A1}$$

The admittances Y_{ijk} contain the transmission-line elements inserted between the transistors' drain terminals and the nodes connecting the linking elements with the capacitive loads Y_{Dk} (Fig. 17). If Y_{Fijk} are the transistors' admittances, Z_{Lk} the characteristic impedances, and θ_{Lk} the electrical lengths of the inserted line transformers, then we obtain the admittances for both tiers $Y_{ijk}^{(A)}$ and $Y_{ijk}^{(B)}$ of the kth active six-port with

$$Y_{11k} = Y_{11Fk} - j\frac{Y_{12Fk}Y_{21Fk}Z_{Lk}\tan\theta_{Lk}}{1 + jY_{22Fk}Z_{Lk}\tan\theta_{Lk}} \tag{A1a}$$

$$Y_{12k} = \frac{Y_{12Fk}}{\cos\theta_{Lk} + jY_{22Fk}Z_{Lk}\sin\theta_{Lk}} \tag{A1b}$$

$$Y_{21k} = \frac{Y_{21Fk}}{\cos\theta_{Lk} + jY_{22Fk}Z_{Lk}\sin\theta_{Lk}} \tag{A1c}$$

$$Y_{22k} = Y_{Dk} + \frac{1}{Z_{Lk}}\frac{Y_{22Fk}Z_{Lk} + j\tan\theta_{Lk}}{1 + jY_{22Fk}Z_{Lk}\tan\theta_{Lk}}. \tag{A1d}$$

The six-port links composed of transmission-line elements are transforming the voltages and the currents in

accordance with

$$\begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ V_{Ck-1} \\ I_{Ck-1} \\ V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = \left[\begin{array}{cc|cc|cc} \cos\theta_{Dk} & jZ_{Dk}\sin\theta_{Dk} & 0 & 0 & 0 & 0 \\ j\frac{1}{Z_D}\sin\theta_{Dk} & \cos\theta_{Dk} & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & \cos\theta_{Ck} & jZ_{Ck}\sin\theta_{Ck} & 0 & 0 \\ 0 & 0 & j\frac{1}{Z_{Ck}}\sin\theta_{Ck} & \cos\theta_{Ck} & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & \cos\theta_{Gk} & jZ_{Gk}\sin\theta_{Gk} \\ 0 & 0 & 0 & 0 & j\frac{1}{Z_{Gk}}\sin\theta_{Gk} & \cos\theta_{Gk} \end{array}\right] \cdot \begin{bmatrix} V_{Dk} \\ -I_{Dk} \\ V_{Ck} \\ -I_{Ck} \\ V_{Gk} \\ -I_{Gk} \end{bmatrix} \tag{A2}$$

In those cases for which the linking elements are inductivities, we have

$$\begin{bmatrix} V_{Dk-1} \\ I_{Dk-1} \\ V_{Ck-1} \\ I_{Ck-1} \\ V_{Gk-1} \\ I_{Gk-1} \end{bmatrix} = \left[\begin{array}{cc|cc|cc} 1 & j\omega L_{Dk} & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 1 & j\omega L_{Ck} & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 1 & j\omega L_{Gk} \\ 0 & 0 & 0 & 0 & 0 & 1 \end{array}\right] \cdot \begin{bmatrix} V_{Dk} \\ -I_{Dk} \\ V_{Ck} \\ -I_{Ck} \\ V_{Gk} \\ -I_{Gk} \end{bmatrix} \tag{A3}$$

If A_I, B_I, C_I, and D_I are the chain parameters of the input matching network and A_O, B_O, C_O, and D_O those of the output matching network, the voltages and currents at the input and output terminals may be calculated with

$$\begin{bmatrix} V_{D0} \\ -Y_D V_{D0} \\ \hline V_{C0} \\ -Y_{CI} V_{C0} \\ \hline V_{G0} \\ I_{G0} \end{bmatrix} = \left[\begin{array}{cc|cc|cc} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & A_I & B_I \\ 0 & 0 & 0 & 0 & C_I & D_I \end{array}\right] \begin{bmatrix} V_{D1} \\ -I_{D1} \\ \hline V_{C1} \\ -I_{C1} \\ \hline V_{G1} \\ -I_{G1} \end{bmatrix} \tag{A4}$$

for the input and with

$$\begin{bmatrix} V_{Dn-1} \\ I_{Dn-1} \\ \hline V_{Cn-1} \\ I_{Cn-1} \\ \hline V_{Gn-1} \\ I_{Gn-1} \end{bmatrix} = \left[\begin{array}{cc|cc|cc} A_O & B_O & 0 & 0 & 0 & 0 \\ C_O & D_O & 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{array}\right] \begin{bmatrix} V_{Dn} \\ -I_{Dn} \\ \hline V_{Cn} \\ Y_{C0}V_{Cn} \\ \hline V_{Gn} \\ Y_G V_{Gn} \end{bmatrix} \tag{A5}$$

for the output terminal.

Finally, the individual 6×6 matrices arranged in the order in which the elementary six-ports are cascaded and multiplied in accordance with (5). This step leads directly to the input and output voltages as well as currents of the matrix amplifier.

The amplifier's idle ports are terminated as shown in Fig. 5. In accordance with the conditions (1c)–(1f), which are reflected in the matrices (A4) and (A5), we are able to reduce the six-port representation of (5) to the more familiar two-port equations (6) that usually characterize an amplifier. The multiplication of the matrices of the elementary six-ports leads us to the six-port matrix that contains the boundary conditions

$$\begin{bmatrix} V_{D0} \\ -Y_D V_{D0} \\ \hline V_{C0} \\ -Y_{CI} V_{C0} \\ \hline V_{G0} \\ I_{G0} \end{bmatrix} = A \begin{bmatrix} V_{Dn} \\ -I_{Dn} \\ \hline V_{Cn} \\ Y_{C0}V_{Cn} \\ \hline V_{Gn} \\ Y_G V_{Gn} \end{bmatrix}. \tag{A6}$$

Here $[A]$ is a 6×6 matrix with the elements A_{ij}. Since (A6) contains all matrix elements A_{ij} of the amplifier, we are now in a position to determine the Y-parameters $Y_{ij}^{(MA)}$ of the ensuing two-port. They are

$$Y_{11}^{(MA)} = \frac{A_{62}\Delta_H + (A_{63} + A_{64}Y_{C0})N_{22} - (A_{65} + A_{66}Y_G)N_{12}}{A_{52}\Delta_H + (A_{53} + A_{54}Y_{C0})N_{22} - (A_{55} + A_{56}Y_G)N_{12}} \tag{A7a}$$

$$Y_{12}^{(MA)} = \left[A_{61} + (A_{63} + A_{64}Y_{C0})\frac{N_{21}}{\Delta_H} - (A_{65} + A_{66}Y_G)\frac{N_{11}}{\Delta_H}\right] - \left[A_{62} + (A_{63} + A_{64}Y_{C0})\frac{N_{22}}{\Delta_H} - (A_{65} + A_{66}Y_G)\frac{N_{12}}{\Delta_H}\right] Y_{22}^{(MA)} \tag{A7b}$$

$$Y_{21}^{(MA)} = \frac{-1}{A_{52} + (A_{53} + A_{54}Y_{C0})\frac{N_{22}}{\Delta_H} - (A_{55} + A_{56}Y_G)\frac{N_{12}}{\Delta_H}} \tag{A7c}$$

and

$$Y_{22}^{(MA)} = \frac{A_{51}\Delta_H + (A_{53} + A_{54}Y_{C0})N_{21} - (A_{55} + A_{56}Y_G)N_{11}}{A_{52}\Delta_H + (A_{53} + A_{54}Y_{C0})N_{22} - (A_{55} + A_{56}Y_G)N_{12}} \quad \text{(A7d)}$$

$$N_{11} = (A_{21} + A_{11}Y_D)H_{22} - (A_{41} + A_{31}Y_{CI})H_{12} \quad \text{(A8a)}$$

$$N_{12} = (A_{22} + A_{12}Y_D)H_{22} - (A_{42} + A_{32}Y_{CI})H_{12} \quad \text{(A8b)}$$

$$N_{21} = (A_{21} + A_{11}Y_D)H_{23} - (A_{41} + A_{31}Y_{CI})H_{13} \quad \text{(A8c)}$$

$$N_{22} = (A_{22} + A_{12}Y_D)H_{23} - (A_{42} + A_{32}Y_{CI})H_{13} \quad \text{(A8d)}$$

$$\Delta_H = H_{13}H_{22} - H_{12}H_{23} \quad \text{(A9)}$$

$$H_{12} = (A_{23} + A_{24}Y_{C0}) + Y_D(A_{13} + A_{14}Y_{C0}) \quad \text{(A10a)}$$

$$H_{13} = (A_{25} + A_{26}Y_G) + Y_D(A_{15} + A_{16}Y_G) \quad \text{(A10b)}$$

$$H_{22} = (A_{43} + A_{44}Y_{C0}) + Y_{CI}(A_{33} + A_{34}Y_{C0}) \quad \text{(A10c)}$$

$$H_{23} = (A_{45} + A_{46}Y_G) + Y_{CI}(A_{35} + A_{36}Y_G). \quad \text{(A10d)}$$

It is immediately obvious from the formulas (A7)–(A10) that only a computer is able to quickly yield reliable results. At this point, as it has become quite common in the analytical treatment, especially of distributed amplifiers, we will for a moment neglect the transistors' feedback ($Y_{F12k} = 0$). This step reduces the expressions (A7) to the comparatively simple equations

$$Y_{11}^{(MA)} = \frac{A_{65} + A_{66}Y_G}{A_{55} + A_{56}Y_G} \quad \text{(A11a)}$$

$$Y_{12}^{(MA)} = 0 \quad \text{(A11b)}$$

$$Y_{21}^{(MA)} = \frac{1}{(A_{55} + A_{56}Y_G)(A_{22} + A_{12}Y_D)} \frac{\Delta_H}{H_{22}} \quad \text{(A11c)}$$

$$Y_{22}^{(MA)} = \frac{A_{21} + A_{11}Y_D}{A_{22} + A_{12}Y_D}. \quad \text{(A11d)}$$

The use of (A11) is, however, only permissible at frequencies where the active devices' internal feedback is negligible. Consequently, at high frequencies, where the use of (A11) may result in significant errors, the accurate formulas (A7), despite their complexity, need to be applied.

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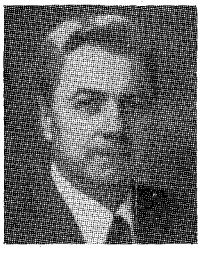

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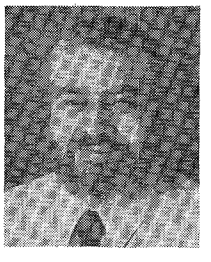
Dr. Niclas is the corecipient of the 1962 Outstanding Publications Award of the German Society of Radio Engineers (NTG) and the 1985 Microwave Prize awarded by the Microwave Theory and Techniques Society of the IEEE.



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